Features

- 3 input reference clocks:
  - Two differential clock pairs supporting up to 3.1GHz and accepting single-ended clock source
  - One crystal input,accepting 8MHz to 50MHz crystal or single-ended clock source
- 10 output clocks:
  - Two power banks with 5 differential outputs each,supporting LVPECL,LVDS and LP_HCSL
  - One independent LVCMOS output clock
- Frequency range:
  - LVCMOS:DC to 350MHz
  - LVDS:DC to 3.1GHz
  - LVPECL:DC to 3.1GHz
  - LP-HCSL:DC to 1GHz
- Excellent Power Supply Ripple Rejection(PSRR)
- Ultra-low latency and skew
- Three independently configurable 1.8V-3.3V power supplies for:
  - Differential outputs
  - Single-ended outputs
  - Core
- Pin-based control,allowing input reference selection,output I/O type selection and output enable/disable
- Working Temperature: -40°C to +85 °C
- Package:48-pin WQFN,7mm x 7mm

General Description

SYKB23F10 is a 3.1GHz high-performance clock fan-out buffer with 10 outputs,designed for low-jitter, high-frequency clock/data distribution and level translation.

The buffer supports clock input selection from either two differential clocks or a crystal input,distributing the selected clock to two output banks,each with five differential outputs,plus one LVCMOS output. Both differential output banks can be configured as LVPECL,LVDS,LP_HSCL,or disabled.

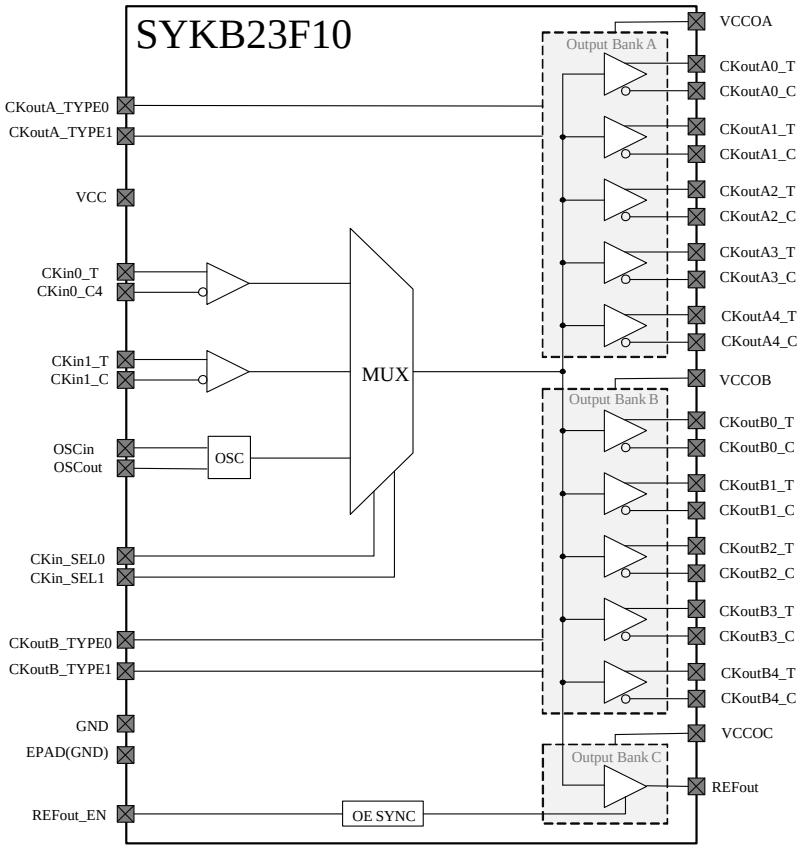
Operating on a core supply of 1.8V-3.3V and three independent output supplies of 1.8V-3.3V, SYKB23F10 provides flexible control via logic pins for input reference selection,differential I/O type selection, and output enable/disable functions.

The buffer can be paired with Montage clock generator SYKG10XX for an effective clock tree solution. Overall,SYKB23F10 offers competitive input reference and output frequency ranges,power strategy,and propagation delay,while supporting a wider working temperature range.

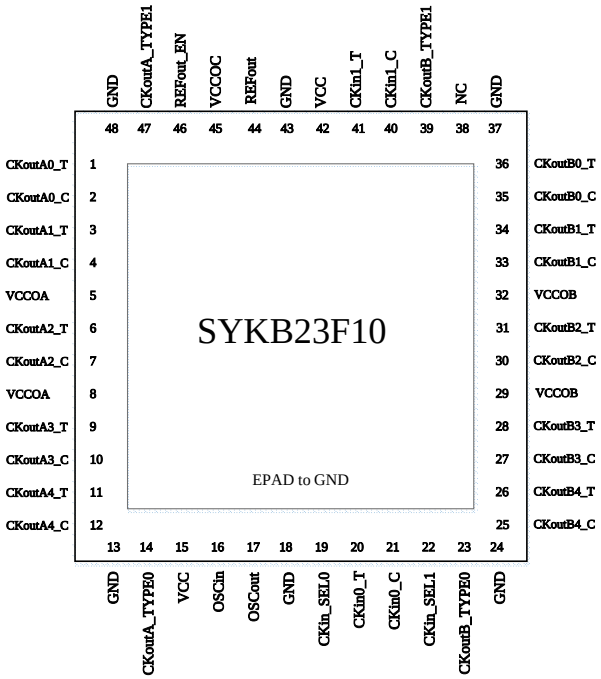
Applications

- Clock distribution and level translation for ADCs, DACs,SATA/SAS,SONET/SDH,multi-gigabit ethernet,and fiber channel line cards
- Servers,storages,switches,routers,and display panels
- PCIe 1.0 to 6.0 and NVLink
- Reference clock distribution for BBU and RRU applications

Functional Block Diagram



Pin Assignment (48-pin WQFN)



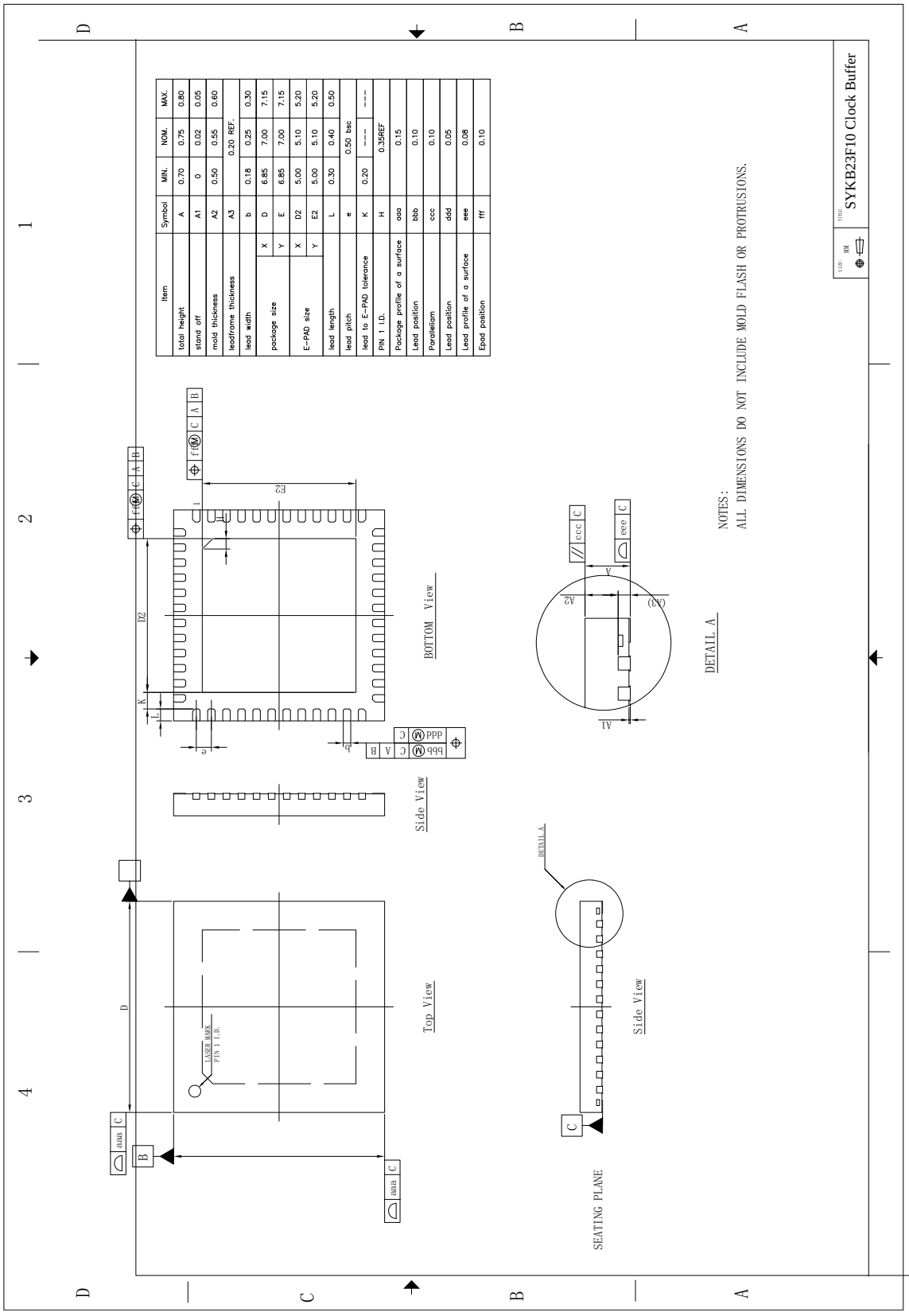
Pin Description

Pin No.	Pin Name	Type[1]	Description
1	CKoutA0_T	O	Differential clock output A0, true port
2	CKoutA0_C	O	Differential clock output A0, complementary port
3	CKoutA1_T	O	Differential clock output A1, true port
4	CKoutA1_C	O	Differential clock output A1, complementary port
5	VCCOA	P	Bank A power supply, 1.8V-3.3V
6	CKoutA2_T	O	Differential clock output A2, true port
7	CKoutA2_C	O	Differential clock output A2, complementary port
8	VCCOA	P	Bank A power supply, 1.8V-3.3V
9	CKoutA3_T	O	Differential clock output A3, true port
10	CKoutA3_C	O	Differential clock output A3, complementary port
11	CKoutA4_T	O	Differential clock output A4, true port
12	CKoutA4_C	O	Differential clock output A4, complementary port
13	GND	P	Ground
14	CKoutA_TYPE0	I	Bank A IO type selection {CKoutA_TYPE1, CKoutA_TYPE0}: • 2’ b00 = LVPECL • 2’ b01 = LVDS • 2’ b10 = LP_HCSL • 2’ b11 = Disabled (HiZ)
15	VCC	P	Core power supply
16	OSCin	I	Crystal in or single-ended clock in
17	OSCout	O	Crystal out or floating if OSCin is used as single-ended clock in
18	GND	P	Ground
19	CKin_SEL0	I	Input reference selection {CKin_SEL1, CKin_SEL0}: • 2’ b00 = CKin0_T & CKin0_C • 2’ b01 = CKin1_T & CKin1_C • 2’ b1x = OSCin
20	CKin0_T	I	Input reference 0, differential-pair (true port) or single-ended
21	CKin0_C	I	Input reference 0, differential-pair (complementary port) or single-ended
22	CKin_SEL1	I	Input reference selection {CKin_SEL1, CKin_SEL0}: • 2’ b00 = CKin0_T & CKin0_C • 2’ b01 = CKin1_T & CKin1_C • 2’ b1x = OSCin
23	CKoutB_TYPE0	I	Bank B IO type selection {CKoutB_TYPE1, CKoutB_TYPE0}: • 2’ b00 = LVPECL • 2’ b01 = LVDS • 2’ b10 = LP_HCSL • 2’ b11 = Disabled (HiZ)

Pin No.	Pin Name	Type1	Description
24	GND	P	Ground
25	CKoutB4_C	O	Differential clock output B4, complementary port
26	CKoutB4_T	O	Differential clock output B4, true port
27	CKoutB3_C	O	Differential clock output B3, complementary port
28	CKoutB3_T	O	Differential clock output B3, true port
29	VCCOB	P	Bank B power supply, 1.8V-3.3V
30	CKoutB2_C	O	Differential clock output B2, complementary port
31	CKoutB2_T	O	Differential clock output B2, true port
32	VCCOB	P	Bank B power supply, 1.8V-3.3V
33	CKoutB1_C	O	Differential clock output B1, complementary port
34	CKoutB1_T	O	Differential clock output B1, true port
35	CKoutB0_C	O	Differential clock output B0, complementary port
36	CKoutB0_T	O	Differential clock output B0, true port
37	GND	P	Ground
38	NC	-	NC
39	CKoutB_TYPE1	I	Bank B IO type selection {CKoutB_TYPE1, CKoutB_TYPE0}: • 2’ b00 = LVPECL • 2’ b01 = LVDS • 2’ b10 = LP_HCSL • 2’ b11 = Disabled (HiZ)
40	CKin1_C	I	Input reference 1, differential-pair (complementary port) or single-ended
41	CKin1_T	I	Input reference 0, differential-pair (true port) or single-ended
42	VCC	P	Core power supply
43	GND	P	Ground
44	REFout	O	Single-ended LVCMOS output
45	VCCOC	P	Bank C (REF) power supply, 1.8V-3.3V
46	REFout_EN	I	REFout enable input, internally synchronized with REFout
47	CKoutA_TYPE1	I	Bank A IO type selection {CKoutA_TYPE1, CKoutA_TYPE0}: • 2’ b00 = LVPECL • 2’ b01 = LVDS • 2’ b10 = LP_HCSL • 2’ b11 = Disabled (HiZ)
48	GND	P	Ground
ePad	GND_EP	P	Exposed pad of package. Connect to ground

1.“ I,” “ O,” and “ P” in this column refer to “ Input” , “ Output,” and “ Power Supply/Ground” , respectively.

Package Outline



Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.70	0.75	0.80
stand off		A1	0	0.02	0.05
mold thickness		A2	0.50	0.55	0.60
leadframe thickness		A3		0.20 REF.	
lead width		b	0.18	0.25	0.30
package size	X	D	6.85	7.00	7.15
	Y	E	6.85	7.00	7.15
E-PAD size	X	D2	5.00	5.10	5.20
	Y	E2	5.00	5.10	5.20
lead length		L	0.30	0.40	0.50
lead pitch		e		0.50 bsc	
lead to E-PAD tolerance		K	0.20	---	---
PIN 1 I.D.		H		0.356EF	
Package profile of a surface		aaa		0.15	
Lead position		bbb		0.10	
Parallelism		ccc		0.10	
Lead position		ddd		0.05	
Lead profile of a surface		eee		0.08	
Epad position		fff		0.10	